Hsu et al.

YOR920030217US1 (RMT)(8728-628)

Fig. 1

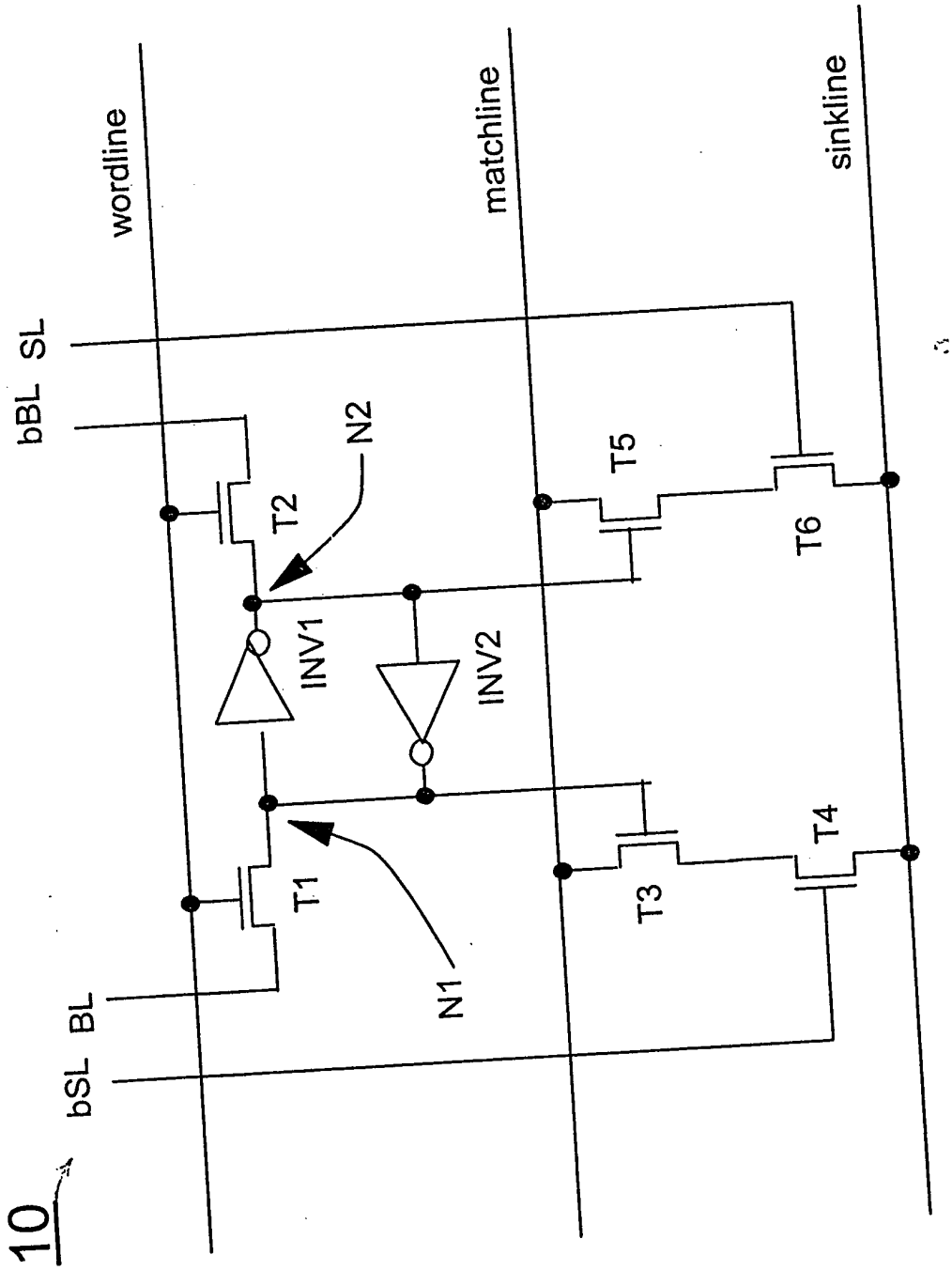
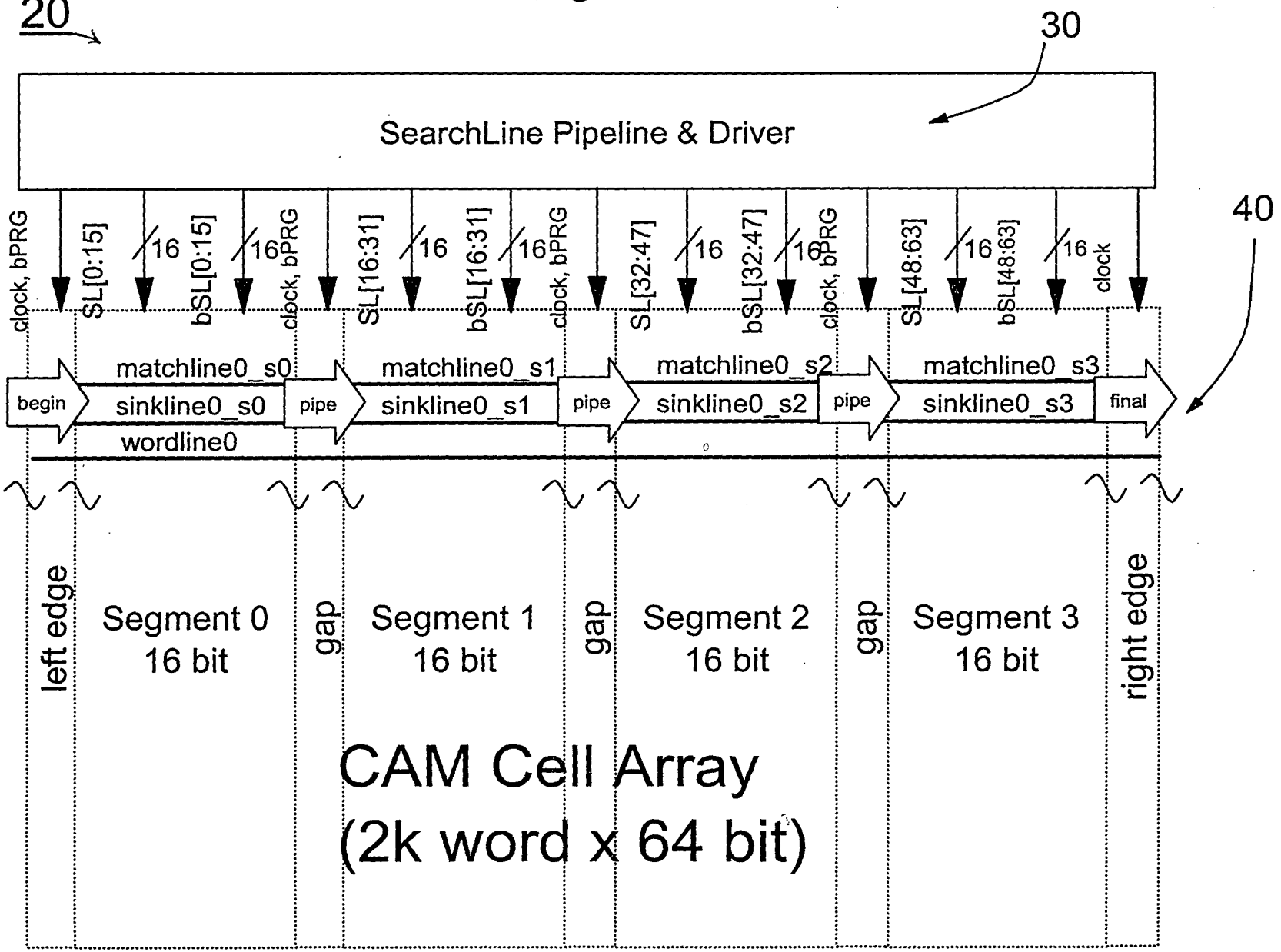


Fig. 2


20
30
SearchLine Pipeline & Driver
40
clock, bPRG
SL[0:15]
16
bSL[0:15]
16
clock, bPRG
SL[16:31]
16
bSL[16:31]
16
clock, bPRG
SL[32:47]
16
bSL[32:47]
16
clock, bPRG
SL[48:63]
16
bSL[48:63]
16
clock
matchline0_s0
matchline0_s1
matchline0_s2
matchline0_s3
begin
sinkline0_s0
pipe
sinkline0_s1
pipe
sinkline0_s2
pipe
sinkline0_s3
final
wordline0
left edge
Segment 0
16 bit
gap
Segment 1
16 bit
gap
Segment 2
16 bit
gap
Segment 3
16 bit
right edge
CAM Cell Array
(2k word x 64 bit)

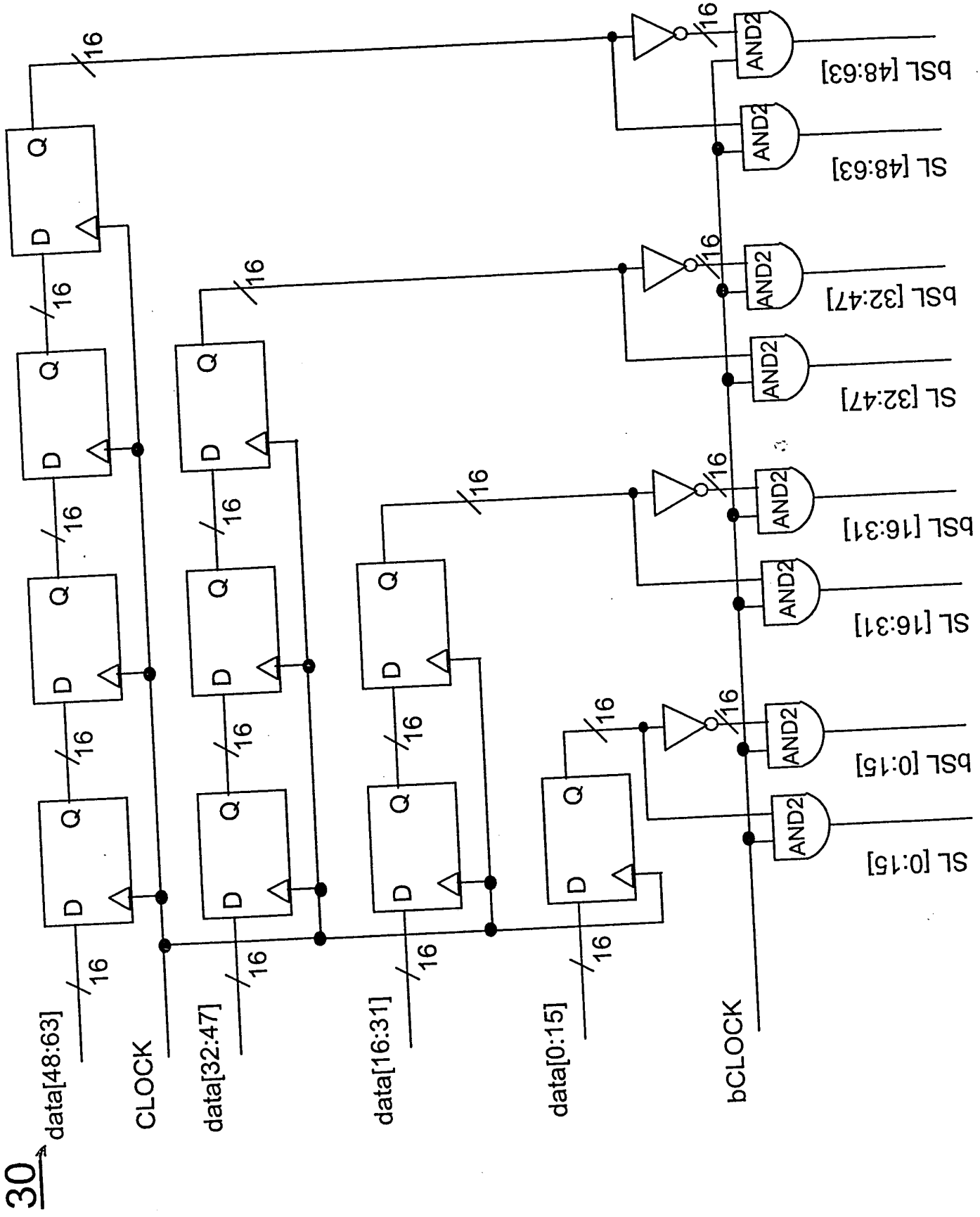


Fig. 3

Fig. 4

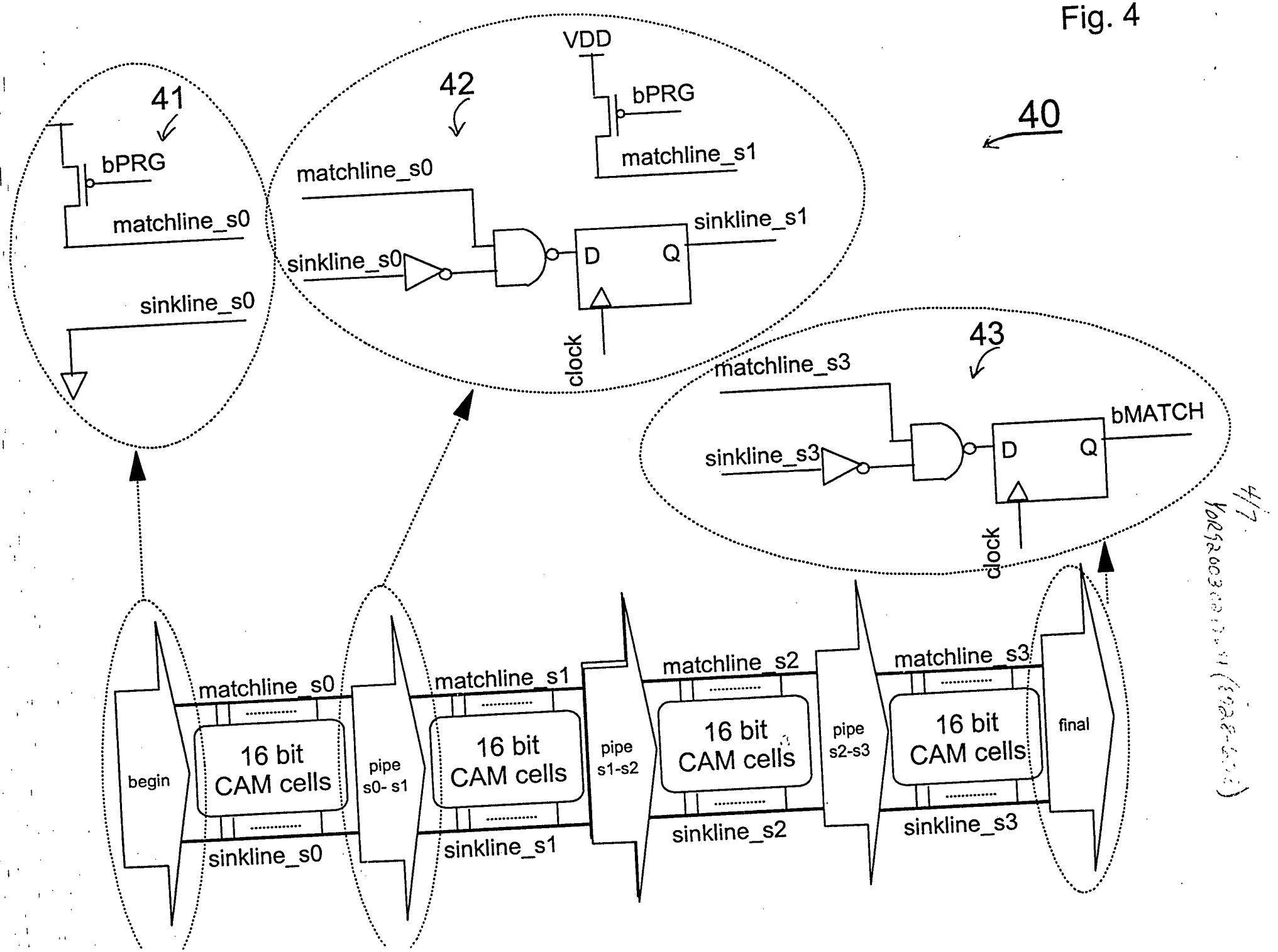

41
bPRG
matchline_s0
sinkline_s0
42
VDD
bPRG
matchline_s1
matchline_s0
sinkline_s1
sinkline_s0
D
Q
clock
40
43
matchline_s3
bMATCH
sinkline_s3
D
Q
clock
begin
matchline_s0
16 bit CAM cells
sinkline_s0
pipe s0- s1
matchline_s1
16 bit CAM cells
sinkline_s1
pipe s1-s2
matchline_s2
16 bit CAM cells
sinkline_s2
pipe s2-s3
matchline_s3
16 bit CAM cells
sinkline_s3
final

Fig. 5

500

	Segment 0 1st clock	Segment 1 2nd clock	Segment 2 3rd clock	Segment 3 4th clock	bMATCH
wordline 0	Sinkline = 0 compare => mismatch	Sinkline = 1 no compare	Sinkline = 1 no compare	Sinkline = 1 no compare	1
wordline 1	Sinkline = 0 compare => match	Sinkline = 0 compare => match	Sinkline = 0 compare => match	Sinkline = 0 compare => mismatch	1
wordline 2	Sinkline = 0 compare => match	Sinkline = 0 compare => mismatch	Sinkline = 1 no compare	Sinkline = 1 no compare	1
wordline 3	Sinkline = 0 compare => mismatch	Sinkline = 1 no compare	Sinkline = 1 no compare	Sinkline = 1 no compare	1
wordline 4	Sinkline = 0 compare => match	Sinkline = 0 compare => match	Sinkline = 0 compare => match	Sinkline = 0 compare => match	0
wordline 5	Sinkline = 0 compare => match	Sinkline = 0 compare => match	Sinkline = 0 compare => mismatch	Sinkline = 1 no compare	1
wordline 6	Sinkline = 0 compare => mismatch	Sinkline = 1 no compare	Sinkline = 1 no compare	Sinkline = 1 no compare	1
.....					

Fig. 6

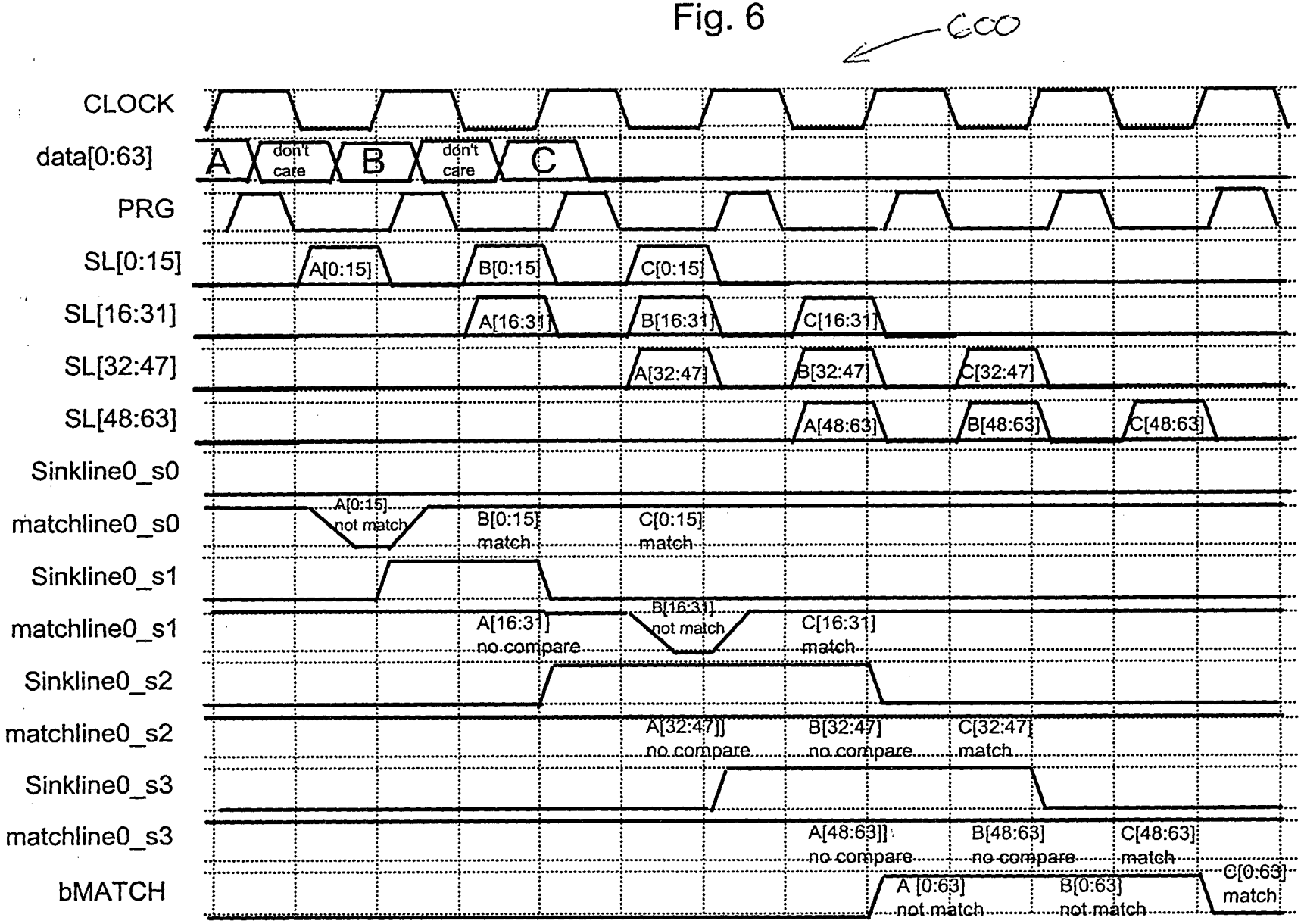

CLOCK
data[0:63]
PRG
SL[0:15]
SL[16:31]
SL[32:47]
SL[48:63]
Sinkline0_s0
matchline0_s0
Sinkline0_s1
matchline0_s1
Sinkline0_s2
matchline0_s2
Sinkline0_s3
matchline0_s3
bMATCH
A
don't care
B
don't care
C
A[0:15]
B[0:15]
C[0:15]
A[16:31]
B[16:31]
C[16:31]
A[32:47]
B[32:47]
C[32:47]
A[48:63]
B[48:63]
C[48:63]
A[0:15] not match
B[0:15] match
C[0:15] match
A[16:31] no compare
B[16:31] not match
C[16:31] match
A[32:47]] no compare
B[32:47] no compare
C[32:47] match
A[48:63]] no compare
B[48:63] no compare
C[48:63] match
A [0:63] not match
B[0:63] not match
C[0:63] match

Fig. 7

700

cases for searchline patterns applied to a word		N-segment architecture Power consumption per cycle			Non-segmented architecture Power consumption per cycle		
		matchline	sinkline	total	matchline	sinkline	total
case 1	continuous all-matching words	0		0	0		0
case 2	alternating between all matching word and 1st seg mismatch	$CV^2/2$	$(N-1)*CV^2/2$	$NCV^2/2$	$NCV^2/2$	0	$NCV^2/2$
case 3	alternating between 1st seg mismatch and last-seg-only mismatch	CV^2	$(N-1)*CV^2/2$	$(N+1)*CV^2/2$	NCV^2	0	NCV^2
case 4	random distributed one-seg-only mismatch	CV^2	~ $NCV^2/6$ for large N	$(1+N/6)CV^2$ for large N	NCV^2	0	NCV^2
case 5	random data	CV^2	~ 0	$\sim CV^2$	NCV^2	0	NCV^2
case 6	mismatch concentrated in one segment	CV^2	~ 0	$\sim CV^2$	NCV^2	0	NCV^2
case 7	random distributed first mismatched seg	CV^2	~ $NCV^2/6$ for large N	$(1+N/6)CV^2$ for large N	NCV^2	0	NCV^2